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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/894,486	06/28/2001	Stephen R. Mooney	884.513US1	5919
21186	7590	05/06/2005	EXAMINER : COX, CASSANDRA F	
SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A. P.O. BOX 2938 MINNEAPOLIS, MN 55402-0938			ART UNIT 2816	PAPER NUMBER

DATE MAILED: 05/06/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

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Office Action Summary

Application No.

09/894,486

Applicant(s)

MOONEY ET AL.

Examiner

Cassandra Cox

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 28 June 2001.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-28 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 10-17 is/are allowed.
- 6) ☒ Claim(s) 1, 18 and 23 is/are rejected.
- 7) ☒ Claim(s) 2-8, 19-22 and 24-28 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 28 June 2001 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date <u>6/28/01</u> . | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claim 1 is rejected under 35 U.S.C. 102(b) as being anticipated by Ojima et al. (U.S. Patent No. 5,608,343).

In reference to claim 1, Ojima discloses in Figure 7 a clock phase interpolator circuit comprising: a first plurality of differential transistor pairs (13, 14, 15, 16), a first plurality of select transistors (17, 18), and a first current source (29), the first current source (29) coupled to each of the first plurality of differential transistor pairs (13, 14, 15, 16) through one of the first plurality of select transistors (17, 18); and a second plurality of differential transistor pairs (21, 22, 23, 24), a second plurality of select transistors (25, 26), and a second current source (32), the second current source (32) coupled to each of the second plurality of differential transistor pairs (21, 22, 23, 24) through one of the second plurality of select transistors (25, 26).

3. Claim 1 is rejected under 35 U.S.C. 102(b) as being anticipated by Satoh et al. (U.S. Patent No. 5,754,062).

In reference to claim 1, Satoh discloses in Figure 15 a clock phase interpolator circuit comprising: a first plurality of differential transistor pairs (T1, T2, T37, T38), a first plurality of select transistors (T9, T10), and a first current source (I21), the first current

source (I21) coupled to each of the first plurality of differential transistor pairs (T1, T2, T37, T38) through one of the first plurality of select transistors (T9, T10); and a second plurality of differential transistor pairs (T5, T6, T15, T16), a second plurality of select transistors (T21, T22), and a second current source (I22), the second current source (I22) coupled to each of the second plurality of differential transistor pairs (T5, T6, T15, T16) through one of the second plurality of select transistors (T21, T22).

Claim 18 is rejected under 35 U.S.C. 102(b) as being anticipated by Applicant's admitted prior art reference Sidiropoulos et al. (A Semidigital Dual Delay-Locked Loop Nov. 1997).

In reference to claim 18, Sidiropoulos discloses in Figure 9 an integrated circuit comprising: a first differential transistor pair to receive a first clock signal at a first phase (ϕ), the first differential transistor pair having a first differential output node (θ); a second differential transistor pair to receive a second clock signal (ψ) at a second phase, the second differential transistor pair having a second differential output node coupled in common with the first differential output node (θ); a first variable current source coupled to the first differential transistor pair; a second variable current source coupled to the second differential transistor pair; and a differential amplifier (shown in Figure 5 as the amplifier and clock buffer receiving the differential output (θ)) having a differential input node coupled to the first differential output node (θ).

In reference to claim 23, Sidiropoulos discloses in Figure 5 the integrated circuit further comprising a delay locked loop (CORE DLL) coupled to the first and second differential transistor pairs (which are part of the phase interpolator and the details of

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which are shown in Figure 9, and which is coupled to the differential transistor pairs through the multiplexers shown in the Figure 5), to provide the first (θ) and second (ψ) clock signals from a received clock signal (In CLK).

Allowable Subject Matter

4. Claims 9-17 are allowed.
5. Claims 2-8, 19-22, and 24-28 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.
6. The following is a statement of reasons for the indication of allowable subject matter: Claims 2-8 would be allowable because the closest prior art of record fails to disclose a circuit as shown in Figure 4 wherein each differential transistor pair (402, 412, 432, 442) is configured to receive a different phase (P0, P1, P2, P3) of a clock signal (CLOCK IN) in combination with the rest of the limitations of the base claims and any intervening claims. Claims 19-22 would be allowable because the closest prior art of record fails to disclose a circuit as shown in Figure 7 wherein the integrated circuit further comprises a third differential transistor pair (706) coupled in parallel with the first differential transistor pair (702) between the first differential output node (710, 711) and the first current source (720) in combination with the rest of the limitations of the base claims and any intervening claims. Claims 24-28 would be allowable because the closest prior art of record fails to disclose a circuit as shown in Figure 1 further comprising a phase detector (130) having input nodes coupled to an output node of the

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differential amplifier (CLOCK OUT) and to a data node (124) in combination with the rest of the limitations of the base claims and any intervening claims.

7. The following is an examiner's statement of reasons for allowance: Claims 9-17 are allowed because the closest prior art of record fails to disclose a circuit as shown in Figure 1 wherein the circuit includes a phase detector (130) and control circuit (140) to compare a phase of a data signal (DATA IN) and a phase of a clock signal on the output clock node (122), and to create interpolator control signals (SEL0-N) and an interpolator circuit (120) operative to switch current responsive to the multiple clock phases (114) and interpolator control signals (142), to drive an output clock (CLOCK OUT) in combination with the rest of the limitations of the base claims and any intervening claims.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Cassandra Cox whose telephone number is 571-272-1741. The examiner can normally be reached on Monday-Thursday from 7:00 AM to 4:30 PM and on alternate Fridays from 7:30 AM to 4:00 PM.

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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 571-272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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April 27, 2005


TIMOTHY P. CALLAHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800